Project Proposal: Design and Verification of 64-Bit Adders

**1. Introduction**

This project proposes the design and verification of three different 64-bit adder architectures. Each adder will utilize a distinct internal implementation approach to explore trade-offs in speed and complexity.

**2. Objectives**

The project aims to achieve the following objectives:

* Design three 64-bit adder models:
  + Ripple Carry Adder (RCA) using full adders
  + Look Ahead Adder (LAA) using 2-bit look ahead modules
  + Behavioral Adder described in Verilog
* Develop a comprehensive test plan for each adder model:
  + Test 1: Iterate through all possible sums from 0 to 31
  + Test 2: Add two large 32-bit numbers

**3. Methodology**

The project will follow these steps for each adder model:

1. **Design:** Create a schematic using structural gate-level components for RCA and LAA models. Implement the behavioral adder in Verilog without specifying the underlying logic circuit.
2. **Simulation:** Simulate each model using appropriate test vectors to validate functionality.
3. **Verification:** Compare simulation results with expected outputs for both test cases.

**4. Deliverables**

The project will deliver the following:

* Verilog code for all three adder models
* Simulation results for each model with both test cases

**5. Project Directory Structure**

The project source code will be organized as follows:

* ripple\_adder\_64: Directory containing the Ripple Carry Adder implementation
* look\_ahead\_adder\_64: Directory containing the Look Ahead Adder implementation
* behavioral\_adder\_64: Directory containing the Behavioral Adder implementation

**6. Conclusion**

This project will provide a comparative analysis of different 64-bit adder implementations. Analyzing the results will offer insights into the trade-offs between speed and complexity associated with each design approach.